REMARKS

Responsive to the Office Action mailed on May 15, 2007 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claims 23-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Claim 27 is withdrawn from consideration.

In this paper, claim 23 is amended to more clearly recite the arrangement of the doped regions of the transistor, the inner landing pad, and the passivation layer. Support for this amendment can be found on page 6, line 25, to page 8, line 9 and FIG. 1I of the application as originally filed. New claims 28-31 are added. Support for the new claims can be found on page 6, line 1, to page 9, line 26 and Figs. 1A-1I of the application as originally filed. Claim 27 is canceled. Thus, on entry of this amendment, claims 23-26 and 28-31 remain in the application.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

Rejections Under 35 U.S.C. 112

Claims 23-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. To the extent that the grounds of the rejections may be applied to the claims now pending in this application, they are respectfully traversed.

On pages 3-4 of the Office Action, the Examiner states that while the amendment filed on March 7, 2007 overcomes the rejections over both Hong and Tu, and no prior art was found after a new search, the limitation "wherein the passivation layer is in contact with the doped region" does not have support in the specification.

As clarified in the instant amendment, claim 23 recites, *inter alia*, a transistor disposed on the substrate, comprising a gate layer covered by a first insulating layer and comprising a ***first*** doped region and a ***second*** doped region, an inner landing pad disposed on the first doped region, and a passivation layer formed on the inner landing pad and in contact with the second doped region.

Support for the amendment is found in an embodiment of the invention described on page 6, line 25, to page 8, line 9 and FIG. 1I of the original application. Namely, doped regions 142 and 144 are formed in the substrate 100 to serve as the source 142 (the second doped region) and the drain 144 (the first doped region), an inner landing pad 112a is disposed on the substrate 110 and drain 144 (the first doped region), and a passivation layer 122 is formed on the inner pad 112a, the transistors 102, and the substrate 100, and is in contact with source 142 (the second doped region). The passivation layer 122 serves to prevent BPSG from diffusing in to the transistor 102 or the substrate 100 (i.e., the substrate 100 comprising the second doped region 142, as shown in 1I). Applicant therefore respectfully requests that the 35 U.S.C. 112 rejection of claim 23 be withdrawn.

Furthermore, for the same reasons advanced by Applicant in connection with the amendment filed on March 7, 2007 and acknowledged by the Examiner in Office action dated May 15, 2007, it is Applicant's belief that there is no teaching or suggestion in the cited art of the claimed arrangement in which a passivation layer is formed on the inner landing pad, the transistor and the substrate, and in contact with the second doped region. For at least this reason, Applicant submits that claim 23 is in condition for allowance. Insofar as claims 24-26 depend from claim 23 either directly or indirectly, it is Applicant's belief that these claims are also in condition for allowance.

New Claims 28-31

New claims 28 recites a structure for a bit line contact hole, comprising:

a substrate;

a transistor, disposed on the substrate, comprising a gate layer covered by a first insulating layer and comprising a first doped region and a second doped region;

an inner landing pad, disposed on the first doped region and parts of the transistor;

a passivation layer, disposed on the inner landing pad, the transistor and the substrate, ***wherein the passivation layer is in contact with the second doped region***;

a second insulating layer, disposed on the passivation layer, having a flat surface on the passivation layer;

a contact plug, disposed on the second insulating layer and the passivation layer, electrically connecting with the inner landing pad; and

an interconnected landing pad, deposited on the contact plug.

For the same reasons discussed in connection with the amendment filed on March 7, 2007 and acknowledged by the Examiner in the Office action dated May 15, 2007, it is Applicant's belief that there is no teaching or suggestion in the cited art of an arrangement in which a passivation layer is formed on the inner landing pad, the transistor and the substrate, and in contact with the second doped region, as recited in claim 28. Applicant therefore submits that claim 28 and claims 29-31 depending there from are in condition for allowance.

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so. The Commissioner is authorized to charge any additional fees that may be required or credit overpayment to Deposit Account No. **502447**.

Respectfully submitted,

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